40193B/54/74C193
4-BIT UP/DOWN BINARY COUNTER

DESCRIPTION — The 40193B is a 4-Bit Synchronous Up/Down Binary Counter. Both operate the same except for the count sequence. Both counters have a Count Up Clock Input (CP_U), a Count Down Clock Input (CP_D), an asynchronous Parallel Load Input ($\overline{PL}$), four Parallel Data Inputs (P_0-P_3), an overriding asynchronous Master Reset (MR), four Counter Outputs (Q_0-Q_3), a Terminal Count Up (Carry) Output ($\overline{TC_U}$) and a Terminal Count Down (Borrow) Output ($\overline{TC_D}$).

When the Master Reset Input (MR) is LOW and the Parallel Load Input ($\overline{PL}$) is HIGH, the Counter Outputs change state on the LOW-to-HIGH transition of either Clock Input. However, for correct counting, both Clock Inputs cannot be LOW simultaneously. With the Master Reset Input (MR) LOW, information on the Parallel Data Inputs (P_0-P_3) is loaded into the counter when the Parallel Load Input ($\overline{PL}$) is LOW and stored in the counter when the Parallel Load Input ($\overline{PL}$) goes HIGH, independent of Clock Inputs (CP_U, CP_D). When HIGH, the Master Reset (MR) resets the counter independent of all other input conditions. See equations below for Terminal Count Outputs ($\overline{TC_U}$, $\overline{TC_D}$).

- **TYPICAL COUNT FREQUENCY OF 8 MHz AT V_{DD} = 10 V**
- **SYNCHRONOUS OPERATION**
- **INTERNAL CASCADING CIRCUITRY PROVIDED**
- **ACTIVE LOW PARALLEL LOAD**
- **ACTIVE HIGH ASYNCHRONOUS MASTER RESET**

PIN NAMES

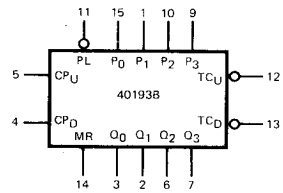
$\overline{PL}$	Parallel Load Input (Active LOW)
P_0-P_3	Parallel Data Inputs
CP_U	Count Up Clock Pulse Input (L→H Edge-Triggered)
CP_D	Count Down Clock Pulse Input (L→H Edge-Triggered)
MR	Master Reset Input (Asynchronous)
Q_0-Q_3	Buffered Counter Outputs
$\overline{TC_U}$	Buffered Terminal Count Up (Carry) Output (Active LOW)
$\overline{TC_D}$	Buffered Terminal Count Down (Borrow) Output (Active LOW)

MODE SELECTION

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

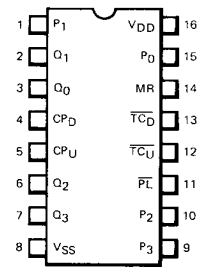
L = LOW Level
H = HIGH Level
X = Don't Care
⎍ = Positive-Going Clock Pulse Edge

LOGIC SYMBOL



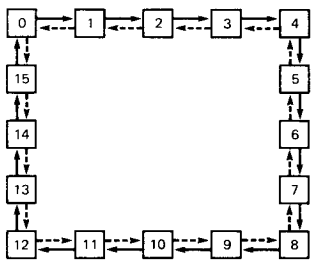
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

40193B STATE DIAGRAM



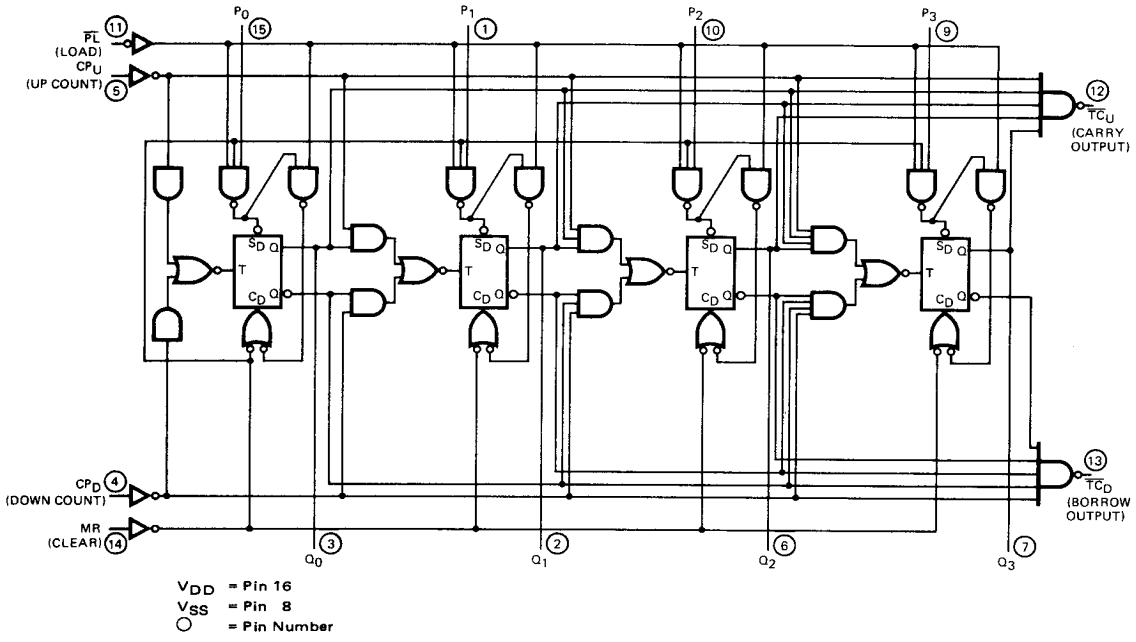
40193B LOGIC EQUATIONS FOR TERMINAL COUNT

Count Up ———
Count Down - - - - - - - - - -

$$TC_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP_U}$$
$$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$$

LOGIC DIAGRAMS

40193B



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_U to Q_n		245	490		105	210		70	175	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			245	490		105	210		70	175		
t_{PLH}	Propagation Delay, CP_D to Q_n		245	490		105	210		70	175	ns	
t_{PHL}			245	490		105	210		70	175		
t_{PLH}	Propagation Delay, CP_U to $\overline{TC_U}$		130	260		60	120		40	96	ns	
t_{PHL}			130	260		60	120		40	96		
t_{PLH}	Propagation Delay, CP_D to $\overline{TC_D}$		145	290		60	120		40	96	ns	
t_{PHL}			145	290		60	120		40	96		
t_{PHL}	Propagation Delay, MR to Q_n		270	540		120	240		80	192	ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ or $\overline{TC_D}$		370	740		170	340		105	270	ns	
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n		270	540		110	220		70	175	ns	
t_{PHL}			270	540		110	220		70	175		
t_{TLH}	Output Transition Time		55	135		30	75		20	45	ns	
t_{THL}			55	135		30	75		20	45		
t_wCP	Min. CP_U or CP_D Pulse Width	170	85		75	30		60	20		ns	
t_wMR	Minimum MR Pulse Width	180	60		80	30		64	20		ns	
$t_w\overline{PL}$	Minimum $\overline{PL}$ Pulse Width	150	75		85	25		52	20		ns	
t_{rec}	MR Recovery Time	150	75		65	30		52	20		ns	
t_{rec}	$\overline{PL}$ Recovery Time	150	75		65	30		52	20		ns	
t_s	Set-Up Time, P_n to $\overline{PL}$	170	85		75	30		60	20		ns	
t_h	Hold Time, P_n to $\overline{PL}$	0	-83		0	-28		0	-19			
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	8		5	12		MHz	

Notes on following page.

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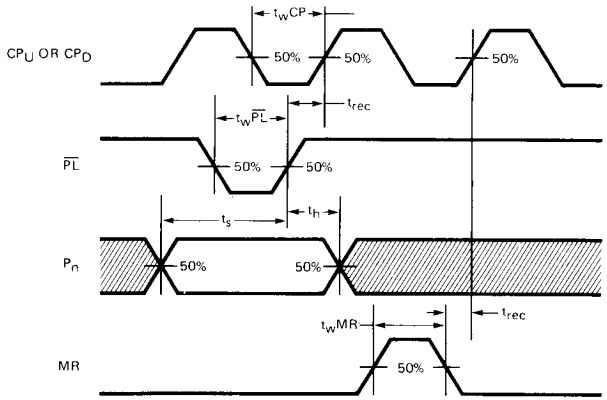
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



RECOVERY TIMES FOR $\overline{PL}$ AND MR, MINIMUM PULSE WIDTHS FOR CP_U, CP_D, $\overline{PL}$ AND MR AND SET-UP AND HOLD TIMES P_n TO $\overline{PL}$

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.