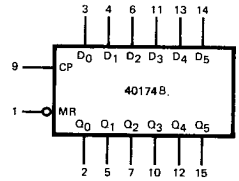
40174B/74C174/54C174
HEX D FLIP-FLOP

DESCRIPTION — The 40174B is a Hex Edge-Triggered D Flip-Flop with six Data Inputs (D_0-D_5), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), and six Buffered Outputs (Q_0-Q_5).

Information on the Data Inputs (D_0-D_5) is transferred to the Buffered Outputs (Q_0-Q_5) on the LOW-to-HIGH transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_5 = LOW) independent of the Clock (CP) and Data Inputs (D_0-D_5). The 40174B is a direct replacement for the 74C174/54C174.

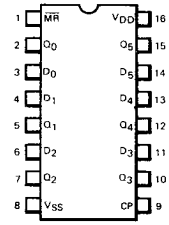
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

CONNECTION DIAGRAM
DIP (TOP VIEW)

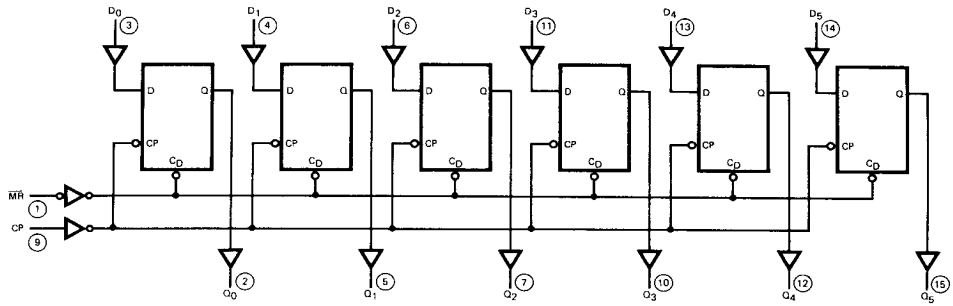


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

D_0-D_5	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_5	Buffered Outputs from the Flip-Flops

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

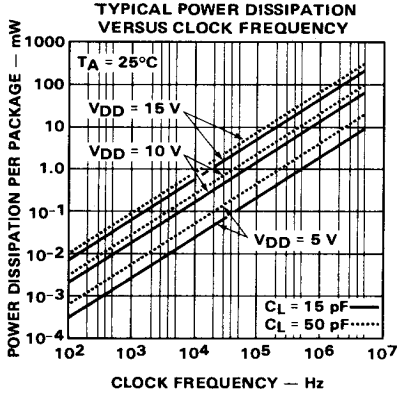
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		70	115		35	60		25	48	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			70	115		35	60		25	48		
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		80	125		40	65		25	52	ns	
t_{TLH}	Output Transition Time		65	135		35	70		15	45	ns	
t_{THL}			65	135		35	70		15	45		
$t_W CP(L)$	Minimum Clock Pulse Width	45	25		20	10		16	8		ns	
$t_W \overline{MR}(L)$	Minimum $\overline{MR}$ Pulse Width	55	35		35	20		28	15		ns	
t_{rec}	$\overline{MR}$ Recovery Time	25	6		13	5		11	2		ns	
t_s	Set-Up Time, D_n to CP	5	1		5	1		4	0		ns	
t_h	Hold Time, D_n to CP	20	10		10	2		8	1			
f_{MAX}	Max. Clock Frequency (Note 3)	5	9		8	16		9	19		MHz	

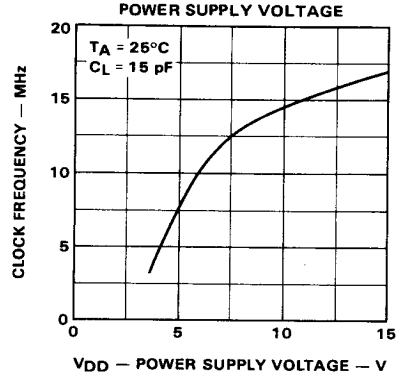
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

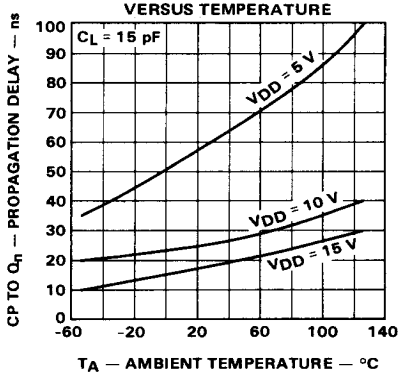
TYPICAL POWER DISSIPATION VERSUS CLOCK FREQUENCY



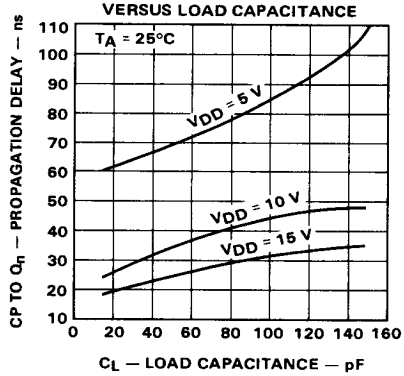
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



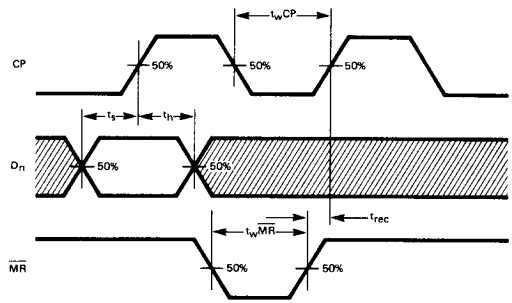
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORM



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$ RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values